ADM-XRC-9R4
User Manual

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1 Introduction

The **ADM-XRC-9R4** is a high-performance XMC for applications using Zynq Ultrascale+ RFSoC DFE from Xilinx.

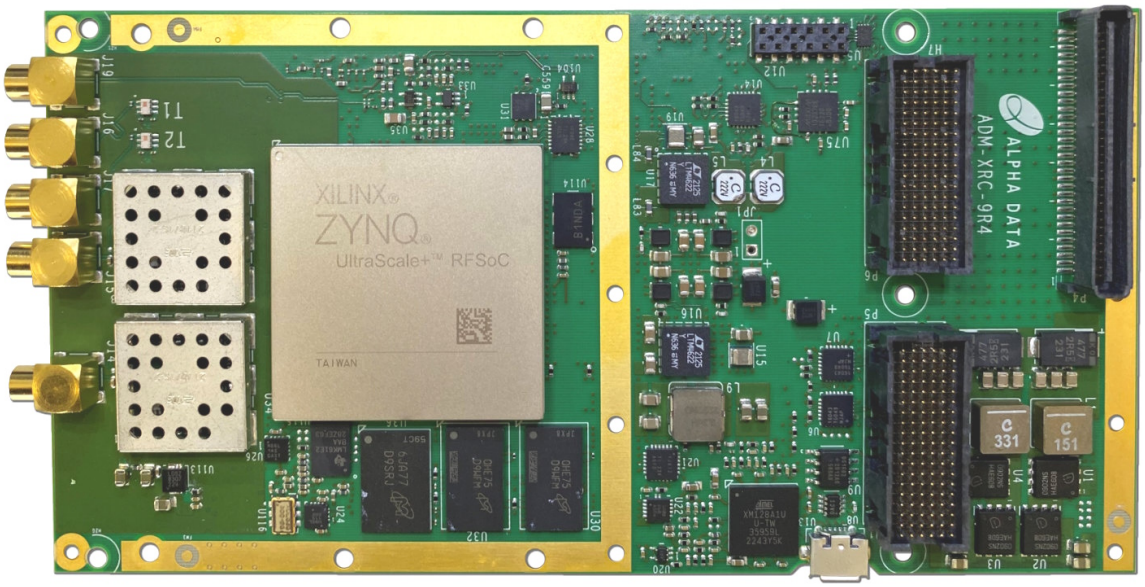

Figure 1 : ADM-XRC-9R4 Board

1.1 Key Features

Key Features

- Single-width XMC, compliant to VITA Standard 42.0 and 42.10d12
- Support for Zynq Ultrascale+ XCZU67DR RFSoC DFE in FFVE1156 packages
- **RF Sampling block consisting of:**
  - 2 14-bit 5.9GSPS RF-ADCs with:
    - Input low-pass filter
    - Fixed amplifier/attenuator
    - 0-31dB Digital Attenuator
    - 450MHz - 2500MHz bandwidth (with default filters/baluns fitted)
    - Full Scale Input (at 2400MHz): 7.0dBm
  - 2 14-bit 10GSPS RF-DACs with:
    - 450MHz - 3100MHz bandwidth (with default baluns fitted\, inverse sinc filter ON)
    - Full Scale Output (800MHz/10GSPS/40.5mA VOP): 3.6dBm
- **Front Panel IO Interface with:**
  - 2 single ended ADC signals
  - 2 single ended DAC signals
  - Reference clock output from RF clocking blocks

- **Processing System (PS) Block consisting of:**
  - Quad-core ARM Cortex-A53, Dual-core ARM Cortex-R5, Mali-400 GPU
  - 1 bank of DDR4-2400 SDRAM 2GB
  - Removable microSD Flash memory
  - Two Quad SPI Flash memory, 512Mb each
  - One serial COM port interfaces to rear P4 connector
  - One system monitor USB port to micro USB connector
- **Programmable Logic (PL) block consisting of:**
  - 8 HSSIO links to the P6 connector
  - 1 banks of DDR4-2400 SDRAM, 1GB per bank
  - 15 3.3V single ended GPIO pins to P6 and P4
  - 20 1.8V single ended or 10 differential GPIO pins to P6
- Voltage and temperature monitoring
- Board management via USB.
- Air-cooled and conduction-cooled configurations

1.2 Order Code

ADM-XRC-9R4/z-y(c)(a)(x)

Name	Symbol	Configurations
Device	z	ZU67
Speed Grade	y	2
Cooling	c	Blank = Air cooled industrial /CC1 = conduction cooled industrial
Coating	a	Blank = No coating /A = Acrylic /A = Polyurethane
XMC Connector	x	Blank = Vita 42 /X2 = Vita 61 connectors /V88 = Vita 88 connectors

Table 1 : Build Options

Not all combinations are available. Please check with Alpha Data sales for details.

1.3 References & Specifications

ANSI/VITA 42.0	*XMC Standard*, December 2008, VITA, ISBN 1-885731-49-3
ANSI/VITA 42.2	*XMC Serial RapidIO Protocol Layer Standard*, Feb 2006, VITA, ISBN 1-885731-41-8
ANSI/VITA 46.9	*PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard*, November 2010, VITA, ISBN 1-885731-63-9
ANSI/IEEE 1386-2001	*IEEE Standard for a Common Mezzanine Card (CMC) Family*, October 2001, IEEE, ISBN 0-7381-2829-5
ANSI/IEEE 1386.1-2001	*IEEE Standard Physical and Environmental Layers for PCI Mezzanine Cards (PMC)*, October 2001, IEEE, ISBN 0-7381-2831-7
ANSI/VITA 20-2001 (R2005)	*Conduction Cooled PMC*, February 2005, VITA, ISBN 1-885731-26-4

Table 2 : References

2 Example Design

An FPGA and PS ARM/Linux example design is available, contact support@alpha-data.com for access. It provides an interactive interface or command line interface to control the board features. It can be used to program the RF clocks, drive signals from the DACs, receive data from the ADCs, control the RF converter settings using the Xilinx XRFDC API and set the DSA attenuation.

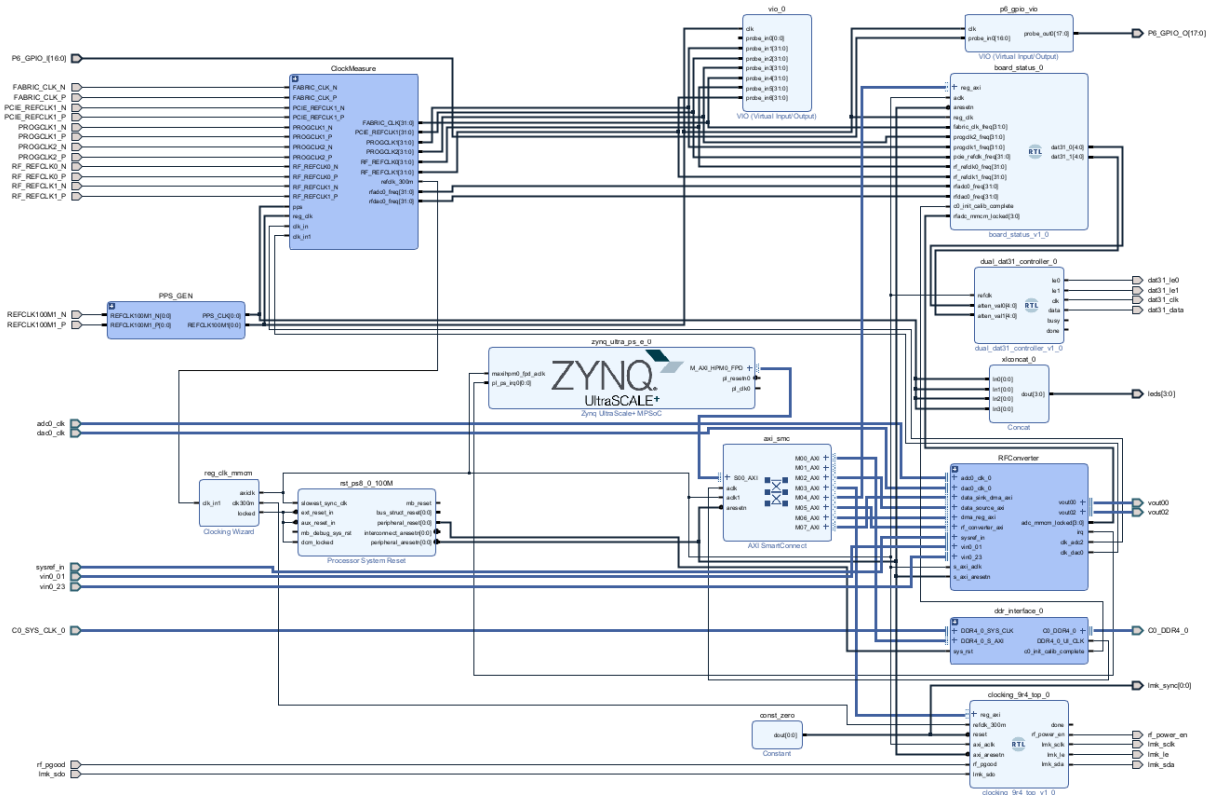

Figure 2 : ADM-XRC-9R4 Vivado Example Design

3 Installation

3.1 Hardware Installation

3.1.1 Handling Instructions

The components on this board can be damaged by electrostatic discharge (ESD). To prevent damage, observe ESD precautions:

- Always wear a wrist-strap when handling the card
- Hold the board by the edges
- Avoid touching any components
- Store in ESD safe bag.

3.1.2 Motherboard / Carrier Requirements

The **ADM-XRC-9R4** is a single width XMC.3 mezzanine with P6 and P4 connectors. The motherboard/ carrier must comply with the XMC.3 specification for the Primary XMC connector, J5.

The Secondary XMC connector, P6 has a pinout compatible with various XMC to VPX signal maps as defined by VITA 46.9. Please consult the pinouts in this user-guide as-well as those of the carrier manufacturer prior to installation. Assistance can be provided by Alpha Data.

The **ADM-XRC-9R4** is compatible with either 5V or 12V on the "VPWR" power rail.

3.1.3 Cooling Requirements

The power dissipation of the board is highly dependent on the Target FPGA application. A power estimator spreadsheet is available on request from Alpha Data. This should be used in conjunction with Xilinx power estimation tools to determine the exact current requirements for each power rail.

The board is supplied with a passive air cooled or conduction cooled heat-sink according to the order number given at time of purchase. It is the users responsibility to ensure sufficient airflow for air cooled applications and metalwork for conduction cooled applications.

The board features system monitoring that measures the board and FPGA temperature. It also includes a self-protection mechanism that will clear the target FPGA configuration if an over-temperature condition is detected.

See Section 4.9 for further details.

4 Functional Description

4.1 Overview

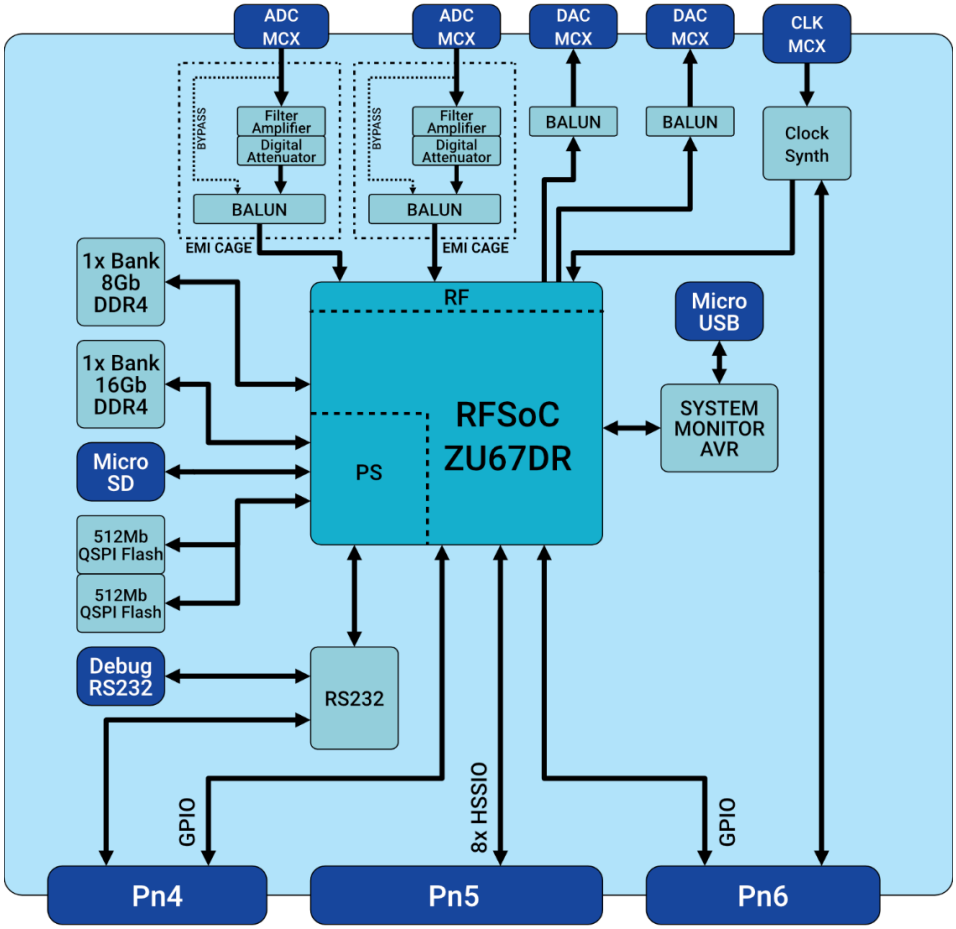

Figure 3 : ADM-XRC-9R4 Block Diagram

4.1.1 Switch Definitions

There is a set of eight DIP switches placed on the rear of the board. Their functions are described in Switch Definitions.

Note:
SW1-5 and SW1-8 are OFF by default. *Factory Configuration* switch must be in the OFF position for normal operation. Other switches can be set as per user requirements.

Switch Ref.	Function	ON State	Off State
SW1-1	BootMode 0	See Table 15	
SW1-2	BootMode 1	See Table 15	
SW1-3	BootMode 2	See Table 15	
SW1-4	BootMode 3	See Table 15	
SW1-5	*Factory Configuration*	-	Normal Operation
SW1-6	XMC JTAG Enable	XMC JTAG interface is enabled	XMC JTAG interface is disabled
SW1-7	XMC PCIE reset enable	Zynq PS will be reset by the XMC PCIE reset signal	Zynq PS will not be reset by the XMC PCIE reset signal
SW1-8	PS Reset	PS is held in reset	Normal Operation

Table 3 : Switch Definitions

4.1.2 LED Definitions

The position and description of the board status LEDs are shown in LED Locations:

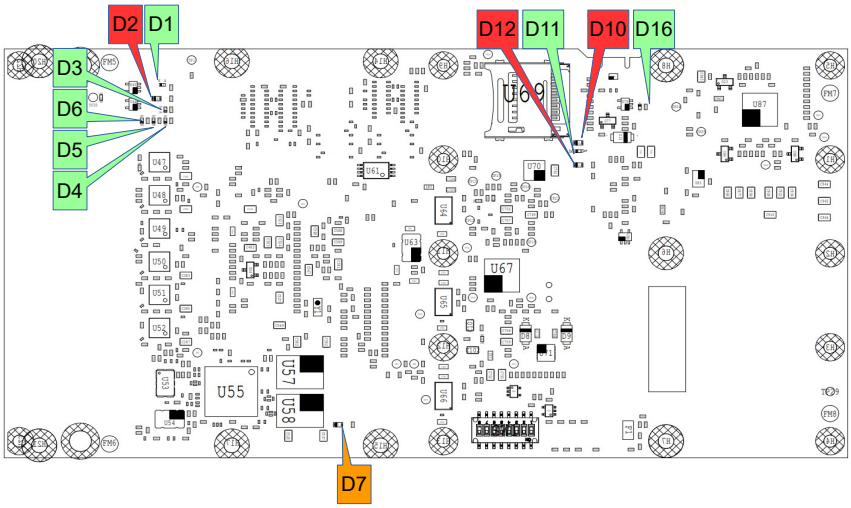

Figure 4 : LED Locations

Comp. Ref.	Function	ON State	Off State
D7(Amber)	MVMRO	Inhibit writes to non-volatile memories	Enable writes to non-volatile memories
D10(Red)	Power Fault	Power supply fault	Normal operation
D11(Green)	Status 0	See Status LED Definitions	
D12(Red)	Status 1	See Status LED Definitions	
D16(Green)	Done	FPGA is configured	FPGA is unconfigured
D2(Red)	PS Error	PS error occurred	No PS error
D1(Green)	PS Status	PS is in secure lockdown state	PS is operating normally
D3(Green)	User LED	Pin high	Pin low
D4(Green)	User LED	Pin high	Pin low
D5(Green)	User LED	Pin high	Pin low
D6(Green)	User LED	Pin high	Pin low

Table 4 : LED Definitions

4.2 XMC Platform Interface

4.2.1 IPMI I2C

A 2 Kbit I2C EEPROM (type M24C02) is connected to the XMC IPMI. This memory contains board information (type, voltage requirements etc.) as defined in the XMC based specification.

4.2.2 MBIST#

Built-In Self Test. This output signal is connected to FPGA pin K10. It is not driven by default.

4.2.3 MVMRO

XMC Write Prohibit. This signal is an input from the carrier. When asserted (high), all writes to non-volatile memories are inhibited. This is indicated by the Amber LED, D9.

The MVMRO signal has a 100KΩ pull-up resistor fitted by default.

This signal cannot be internally driven or over-ridden. A buffered version of the signal is connected to the PS at pin K19.

4.2.4 MRSTI#

XMC Reset In. This signal is an active low input from the carrier. A this signal connected to the PS at pin G21. This signal can also drive the PS power-on-reset pin depending on SW1-7

A buffered version of MRSTI# is also connected to the FPGA at pin J12.

4.2.5 MRSTO#

XMC Reset Out. This optional output signal is driven from the FPGA pin K12.

4.2.6 MPRESENT#

Module Present. This output signal is connected directly to GND.

4.3 JTAG Interface

4.3.1 On-board Interface

A JTAG boundary scan chain is connected to header U12. This allows the connection of the Xilinx JTAG cable for FPGA debug using the Xilinx ChipScope tools.

The scan chain is shown in JTAG Boundary Scan Chain:

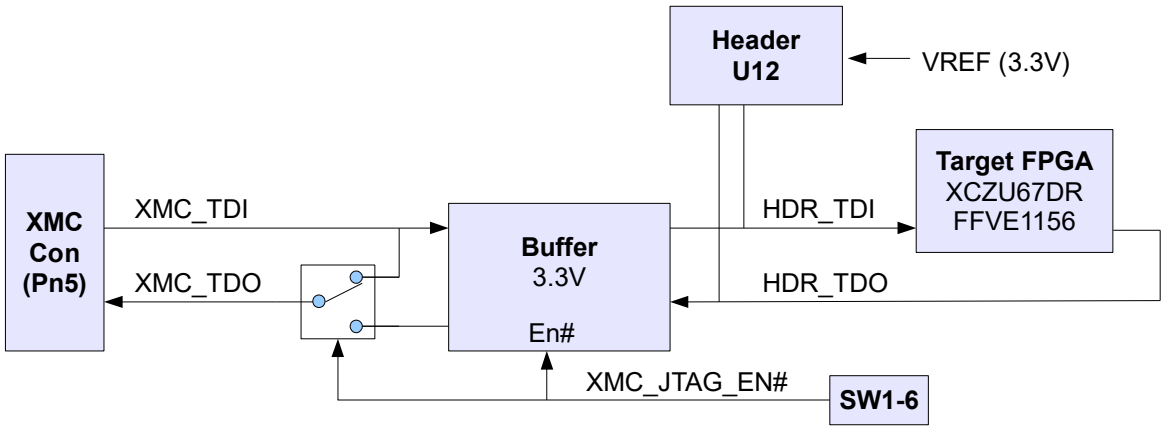

Figure 5 : JTAG Boundary Scan Chain

> **Note:**
> If the JTAG chain is connected to the interface at the XMC connector (SW1-6 is ON), Header U12 should not be used.

4.3.2 XMC Interface

The JTAG interface on the XMC connector is normally unused and XMC_TDI connected directly to XMC_TDO.

The interface can be connected to the on-board interface (through level-translators) by switching SW1-6 ON. See Switch Definitions

4.3.3 JTAG Voltages

The on-board JTAG scan chain uses 3.3V. The Vcc supply provided on U12 to the JTAG cable is +3.3V and is protected by a poly fuse rated at 350mA.

The JTAG signals at the XMC interface use 3.3V signals and are connected through level translators to the on-board scan chain.

4.4 Clocks

The **ADM-XRC-9R4** provides a wide variety of clocking options. The board has a user-programmable clock generator. These clocks can be combined with the FPGA's internal PLLs to suit a wide variety of communication protocols.

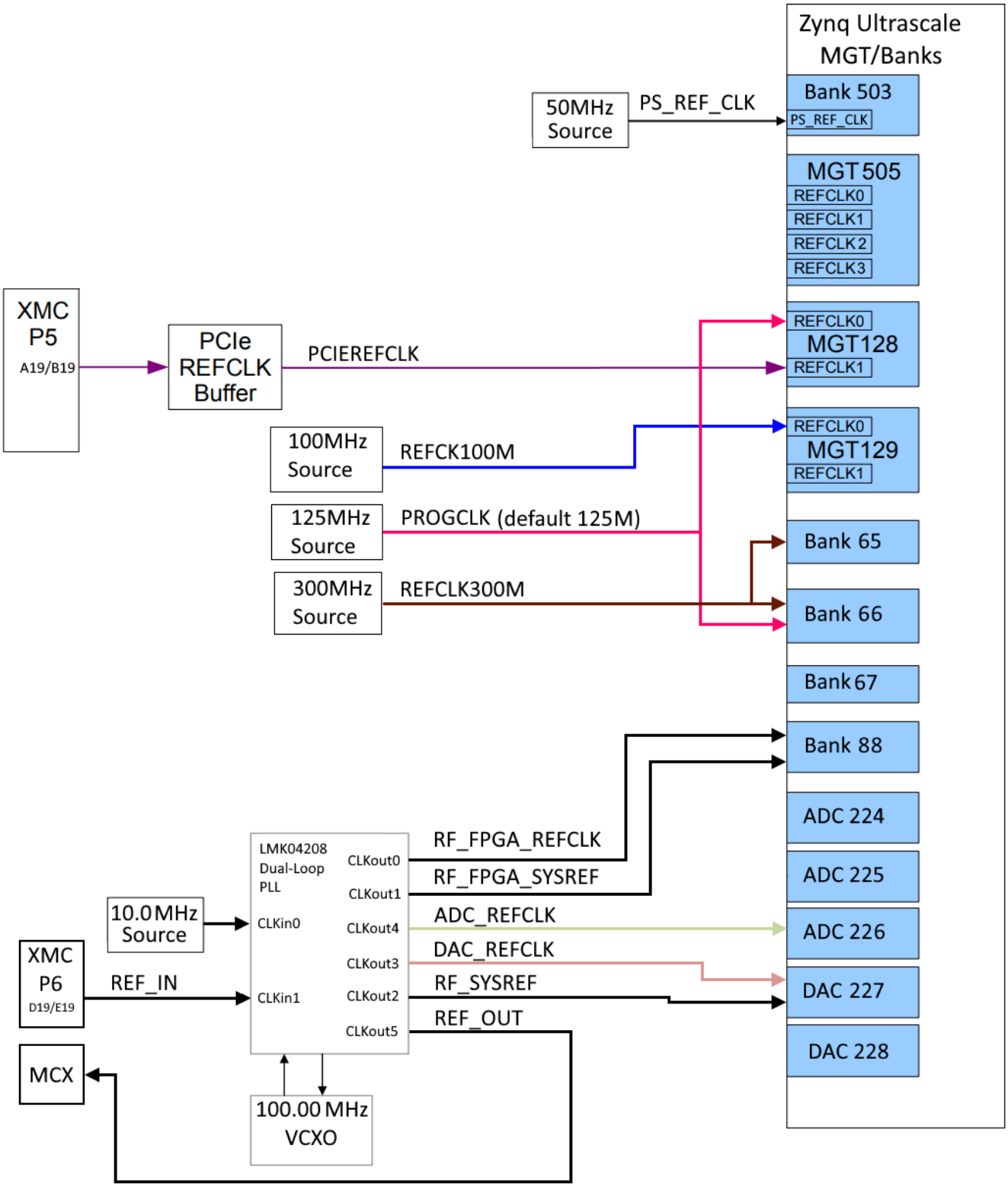

Figure 6 : Full Clock Diagram

4.4.1 300MHz Reference Clocks (REFCLK300M and FABRIC_CLK)

The fixed 300MHz reference clocks REFCLK300M and FABRIC_CLK are differential LVDS signals.

REFCLK300M is used as the input clock for both DDR4 SDRAM interfaces.

FABRIC_CLK is used as the reference clock for the IO delay control block (IDELAYCTRL).

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK300M	300 MHz	IO_L11_T1U_N8_GC_65	LVDS	AJ16	AJ15
FABRIC_CLK	300 MHz	IO_L14_T2L_N2_GC_66	LVDS	AM12	AM11

Table 5 : REFCLK300M Connections

4.4.2 100MHz Reference Clocks (REFCLK100M)

The fixed 100MHz reference clock REFCLK100M are differential LVDS signals.

REFCLK100M is used as the reference clock for the PL MGT banks.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
REFCLK100M	100 MHz	MGTREFCLK0_127	LVDS	M28	M29

Table 6 : REFCLK100M Connections

4.4.3 PCIe Reference Clocks (PCIEREFCLK)

The 100MHz PCI Express reference clock is provided by the carrier card through the Primary XMC connector, P5 at pins A19 and B19. This clock is buffered into two PCIe Express reference clocks that are forwarded to the PS GTR and PL GTY transceivers.

Signal	Frequency	FPGA Input	IO Standard	"P" pin	"N" pin
PCIEREFCLK	100 MHz	MGTREFCLK1_128	LVDS	F28	F29

Table 7 : PCIEREFCLK Connections

4.4.4 Programmable Clocks (PROGCLK 0-2)

There is one programmable clock source that is forwarded throughout the FPGA. This clock is programmable through the USB system monitor. PROGCLK[2:1] is generated by a dedicated programmable clock generator IC and offer extremely high frequency resolutions (1ppm increments). PROGCLK[2:1] are all buffered copies of the same clock signal.

Contact support@alpha-data.com for details on re-programming this clock.

Signal	Frequency	Target FPGA Input	IO Standard	"P" pin	"N" pin
PROGCLK1	10 - 1000 MHz	MGTREFCLK0_128	LVDS	H28	H29
PROGCLK2	10 - 1000 MHz	IO_L13_T2L_N0_G-C_QBC_66	LVDS	AL9	AM9

Table 8 : PROGCLK Connections

4.4.5 MGT Reference Clocks

The PS and PL MGTs can be clocked by sources from the P5, P6 or on-board clock sources

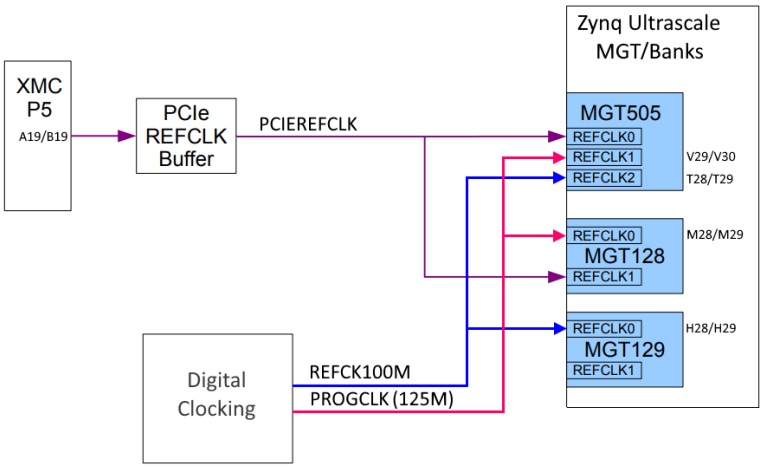

Figure 7 : MGT Clocks

4.4.6 PS System Clock

There PS is clocked by a fixed oscillator.

Signal	Frequency	FPGA pin
PS Ref Clock	50MHz	M25

Table 9 : PS System Clock Connections

4.4.7 RF Sampling Clocks

The RF reference clocks are generated with a dual-loop jitter cleaner PLL. The RF sampling clocks are using the on-chip PLLs in the RFSoC.

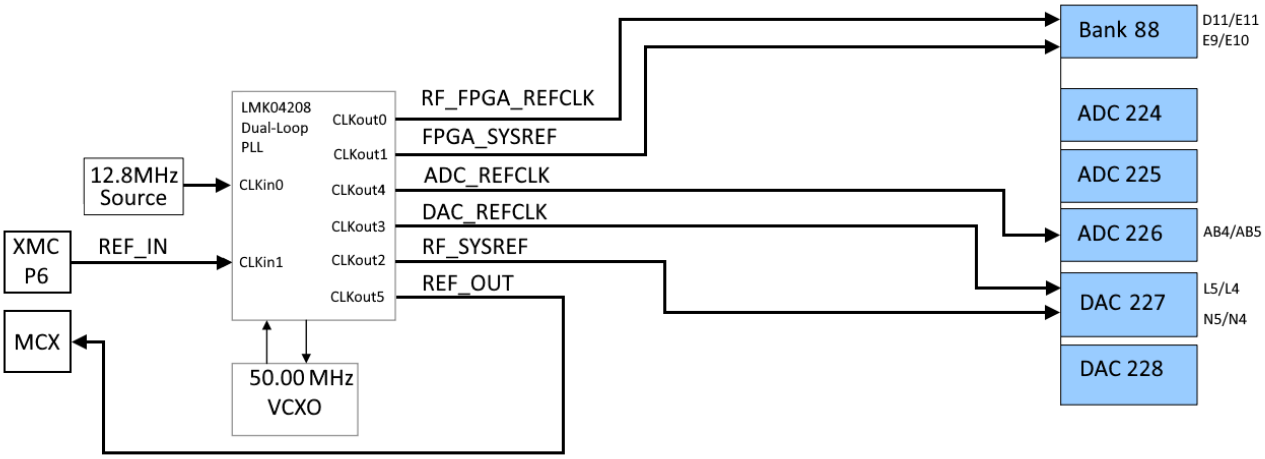

Figure 8 : ADM-XRC-9R4 RF sampling clocks

Source	Frequency
External Reference Clock	0.1 - 500MHz
On-Board Reference Clock	12.80MHz
VCXO	50.00MHz

Table 10 : RF Clock Sources

Signal	Frequency	Target FPGA Input	"P" pin	"N" pin
ADC_REFCLK	Variable	ADC_CLK_226	AB5	AB4
DAC_REFCLK	Variable	DAC_CLK_227	L5	L4

Table 11 : RF Clock Connections

4.4.7.1 Sysref Clocks

The sysref clocks provide the sysref functionality to synchronize the RF DACs and ADCs. They are provided by the RF clock generators. They are connected to the PL and the RF sampling block.

Signal	Frequency	Target FPGA Input	"P" pin	"N" pin
FPGA Sysref Clock	Variable	IO_L11_T1U_N9_GC_66	AM10	AN10
RF Sysref Clock	Variable	SYSREF_227	N5	N4

Table 12 : SysRef Connections

4.4.7.2 RF System FPGA Reference Clock

The RF system FPGA reference clock is a differential clock signal from the RF clock generation circuit, and is connected to a GC input on the PL.

Signal	Frequency	Target FPGA Input	"P" pin	"N" pin
RF System FPGA Reference Clock	Variable	IO_L11_T1U_N8_GC_66	AP11	AP10

Table 13 : FPGA Reference Clock Connections

4.4.7.3 RF Clock Programming

The RF reference clocks are programmed from the PL using uWire. Both writing and readback are supported.

Signal	FPGA Pin	IO Standard	Description
LMK_CLK	AP7	LVCMOS18	uWire interface clock
LMK_LE	AP8	LVCMOS18	uWire interface chip select
LMK_SDA	AP6	LVCMOS18	uWire interface data to device (from FPGA)
LMK_STAT_LD	AP5	LVCMOS18	uWire interface data from device (to FPGA)
LMK_SYNC	AM6	LVCMOS18	LMK04208 sync pin
RF_POWER_EN	AN5	LVCMOS18	Power good signal from RF power supplies.
RF_PGOOD	AM5	LVCMOS18	Power good signal from RF power supplies.

Table 14 : FPGA 4-Wire Connections

4.5 Zynq PS Block

4.5.1 Boot Modes

BootMode0 (SW1-1)	BootMode1 (SW1-2)	BootMode2 (SW1-3)	BootMode3 (SW1-4)	Boot Mode
ON	ON	ON	ON	JTAG
ON	OFF	ON	ON	Quad SPI
OFF	OFF	ON	ON	SD Flash
-	-	-	-	Reserved

Table 15 : Boot Mode Selection

4.5.2 Quad SPI Flash Memory

1Gb Flash Memory (2x Micron MT25QU512AB) is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream. The QSPI memory uses the dual-parallel configuration

The flash memory can only be accessed by the PS. Utilities for erasing, programming and verification of the flash memory are available in Linux.

4.5.3 MicroSD Flash Memory

A MicroSD card is used for storing executable code and data for the PS and PL, such as a bootloader, operating system and bitstream.

The flash memory can only be accessed by the PS.

4.5.4 PS DDR4 Memory

The **ADM-XRC-9R4** is fitted with one bank of PS DDR4 SDRAM. The bank is made up of a two 16-bit wide memory devices in parallel to provide a 32-bit datapath capable of running up to 1200MHz (DDR4-2400). 8Gbit devices (Micron MT40A512M16HA-083) are fitted as standard to provide 2GByte of memory.

Full details of the interface, signaling standards and an example design are provided in the ADM-XRC-9R4 example design.

4.5.5 PS MGT Links

The PS MGT links are unconnected on this board

4.5.6 Serial COM Ports

There is one RS232 serial COM port connected to PMC connector P4 and P6, as shown in Figure Serial COM Ports. The default speed of the COM ports is 115.2k.

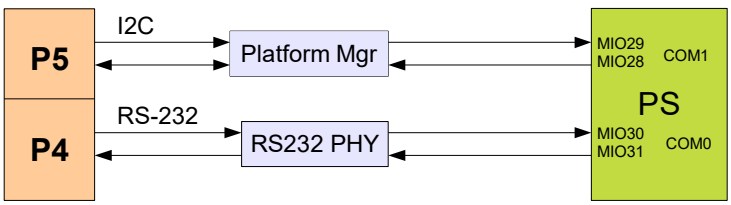

Figure 9 : Serial COM Ports

4.6 PL Interfaces

4.6.1 I/O Bank Voltages

The Target FPGA IO is arranged in banks, each with their own supply pins. The bank numbers, their voltage and function are shown in Target FPGA IO Banks. Full details of the IOSTANDARD required for each signal are given in the ADM-XRC-9R4 example design.

IO Banks	Voltage	Purpose
503	3.3V	Configuration, JTAG, Boot Mode Select
88	3.3V	PN4/PN6 single ended GPIO
66	1.8V	PN6 differential GPIO
65	1.2V	DRAM Bank 0

Table 16 : Target FPGA IO Banks

4.6.2 MGT Links

There are a total of 8 Multi-Gigabit Transceiver (MGT) links connected to the Target FPGA:

Links	Width	Connection
P5(7:0)	8	Direct link to XMC P5 lanes (7:0)

Table 17 : Target MGT Links

The connections of these links are shown in MGT Links:

For MGT Clocking see MGT Clocks:

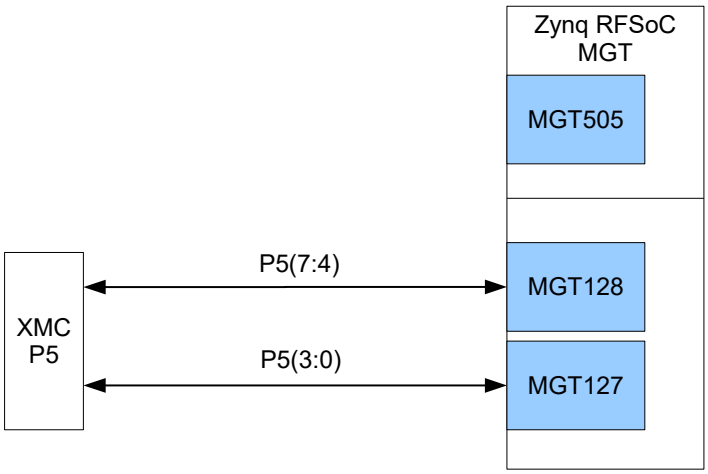

Figure 10 : MGT Links

4.6.3 Memory Interfaces

The **ADM-XRC-9R4** has one banks of PL DDR4 SDRAM. The bank consists of one 8-bit wide memory device capable of running at up to 1200MHz (DDR-2400). 8Gbit devices (Micron MT40A1G8PM-083E) are fitted as standard.

The memory bank is arranged for compatibility with the Xilinx Memory Interface Generator (MIG). PL DRAM Banks shows the component references and FPGA banks used. Full details of the interface, signalling standards and an example design are provided in the ADM-XRC-9R4 example design.

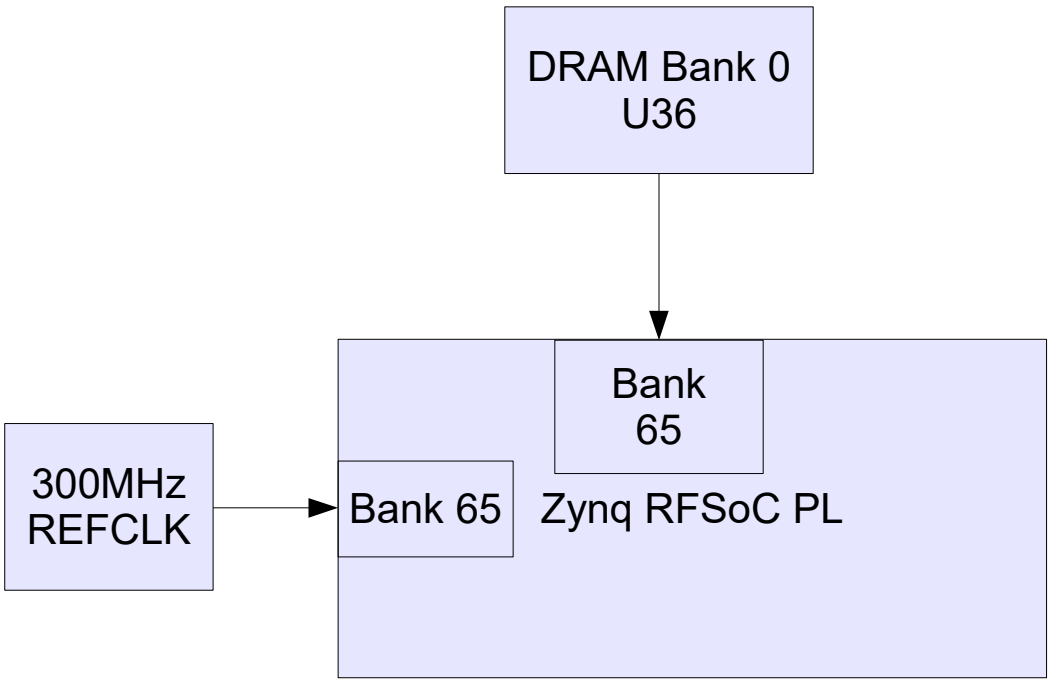

Figure 11 : PL DRAM Banks

4.6.4 GPIO

There are 15 3.3V GPIO pins and 10 1.8V differential pairs from the FPGA.

The GPIO pin mapping is shown in Pn6 GPIO Pin Map.

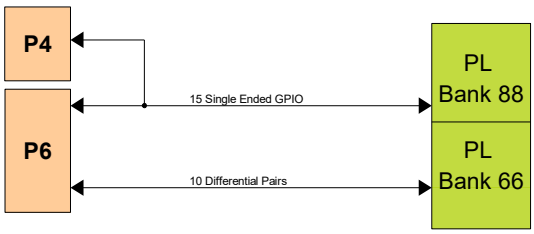

Figure 12 : GPIO Block Diagram

4.7 RF Interfaces

4.7.1 Front-Panel I/O

The front panel interface consists of 5 MCX connectors J14, J15, J16, J17 and J19.

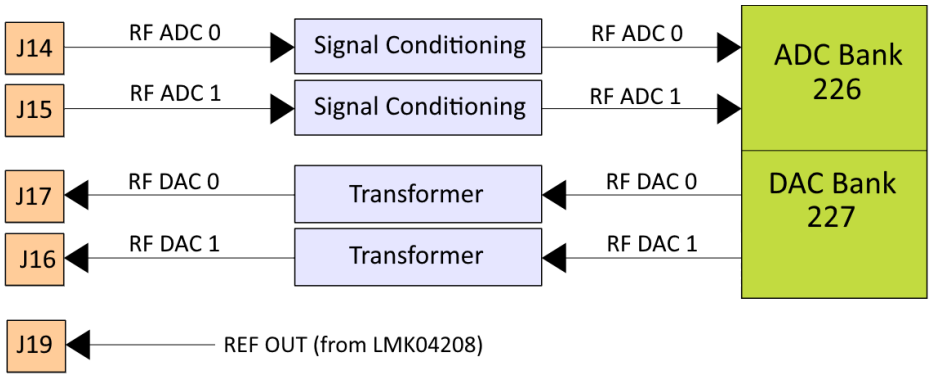

Figure 13 : Front Panel RF IO

Figure 14 : ADC Signal Path

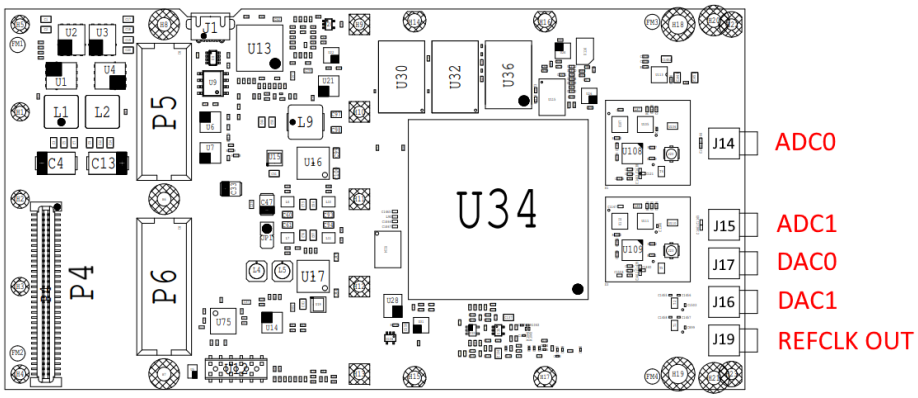

Figure 15 : Front Panel Pinout

The ADC voltages in the table below are the single ended voltages at the RF connector. The DAC voltages are the voltages driving a 50 Ohm impedance.

Signal	Impedance (Ohms)	Connector	FPGA Pin
ADC0	50	J14	Y4/Y5
ADC1	50	J15	V4/V5
DAC0	50	J17	N2/N1
DAC1	50	J16	L2/L1
REF OUT	50	J19	-

Table 18 : Front panel I/O signals

4.7.2 RF Performance

4.7.2.1 ADC RF Performance

Measurement	Conditions/Comments	Value	Unit
Resolution		14	Bits
Sample Rate		1.0 - 5.9	GS/s
Full Scale Input	DSA attenuation = 0dB	1.4	Vpk-pk
Full Scale Input	DSA attenuation = 0dB	7.0	dBm
1dB compression (p1dB)	DSA attenuation = 0dB	0.55	dBm
Third order intercept (ip3)	DSA attenuation = 0dB	17.3	dBm
ADC0 to ADC1 Crosstalk	0dB attenuation, 2600MHz	-80.5	dBm
ADC0 to ADC1 Crosstalk	0dB attenuation, 2200MHz	-82.8	dBm
SNR	0dB Atten, 2400MHz, -18dBm input	50.1	dBm
SFDR	0dB Atten, 2400MHz, -18dBm input	60.8	dBm
ADC0 Received Power	0dB Atten, 2400MHz, -18dBm input	18.98	dBm
ADC1 Received Power	0dB Atten, 2400MHz, -18dBm input	18.90	dBm
ADC0 to ADC1 phase	0dB Atten, 2400MHz, -10dBm input	-1.55	degrees
ADC0 to ADC1 delay	0dB Atten, 2400MHz, -10dBm input	-1.79	ps

Table 19 : ADC Parameters

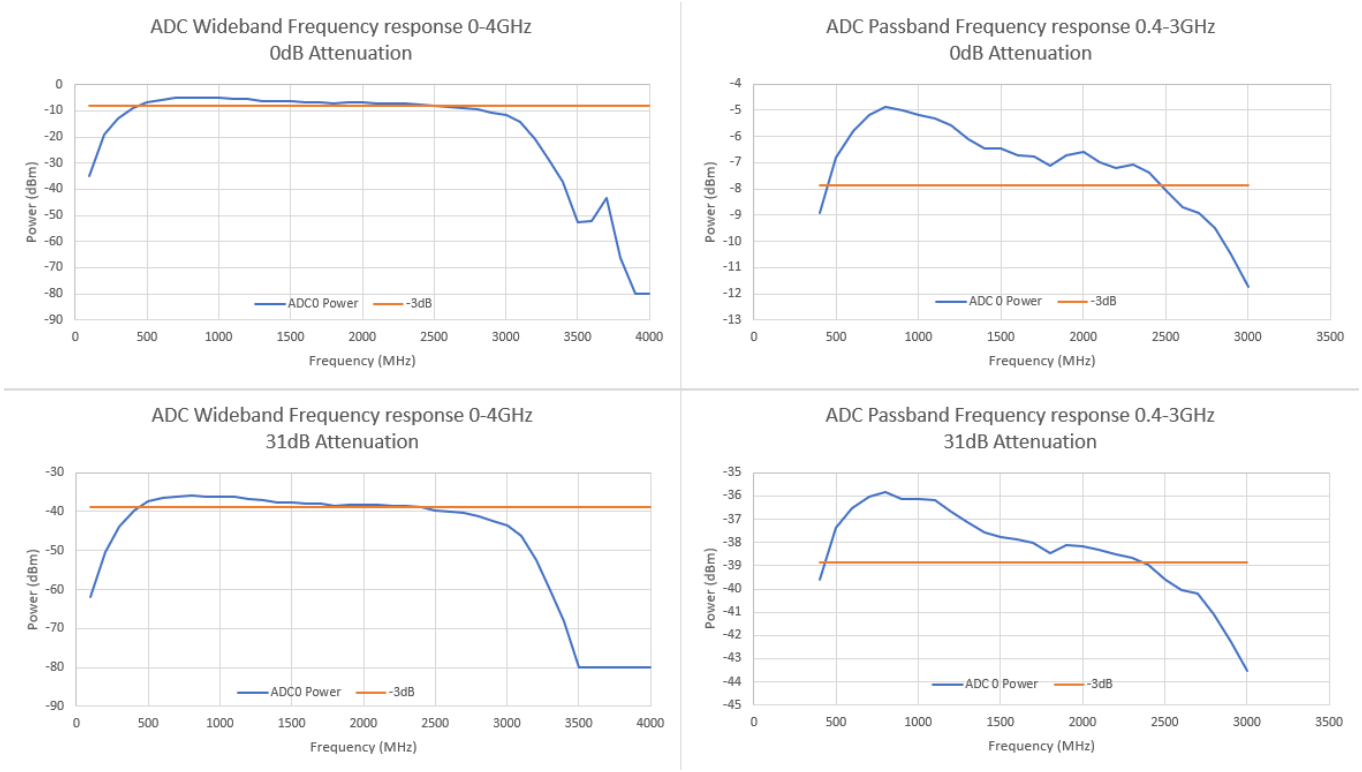

Figure 16 : ADM-XRC-9R4 ADC Frequency Response

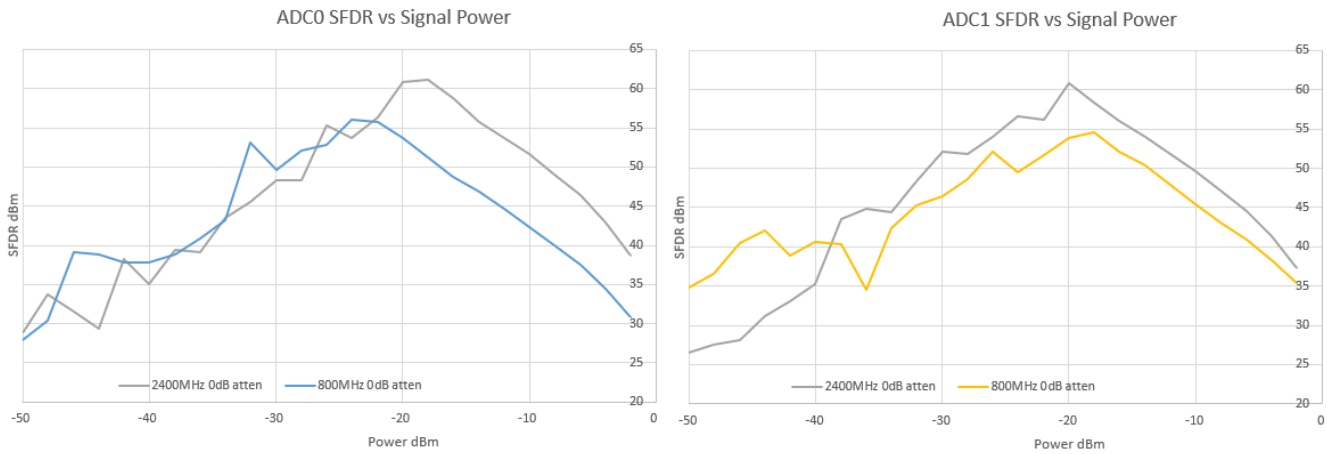

Figure 17 : ADM-XRC-9R4 ADC SFDR vs Signal Power

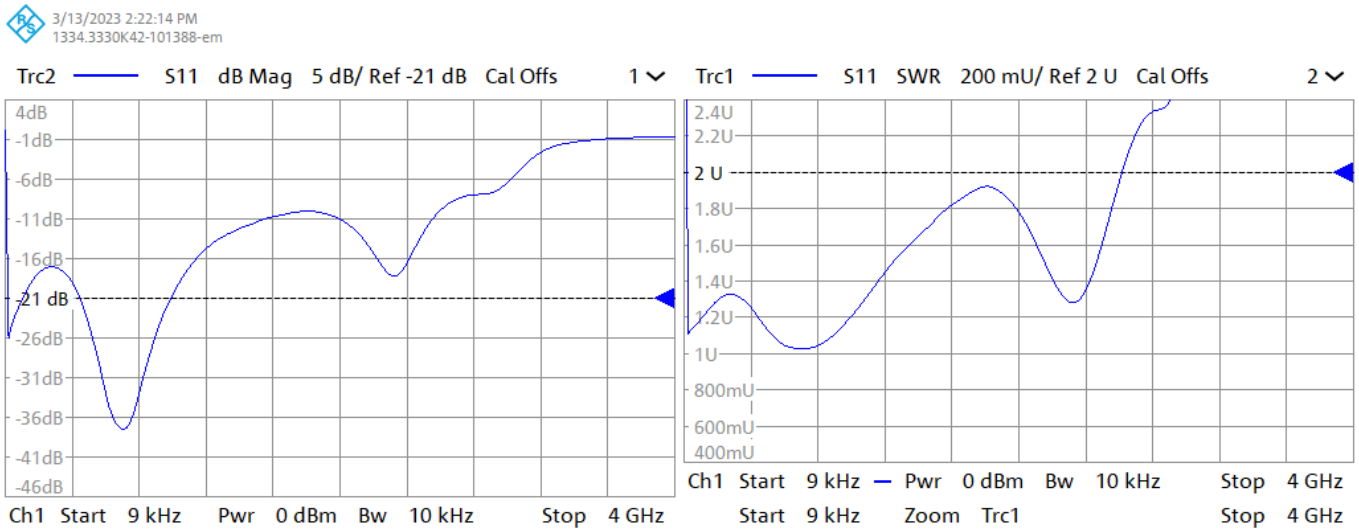

Figure 18 : ADM-XRC-9R4 ADC Input Matching

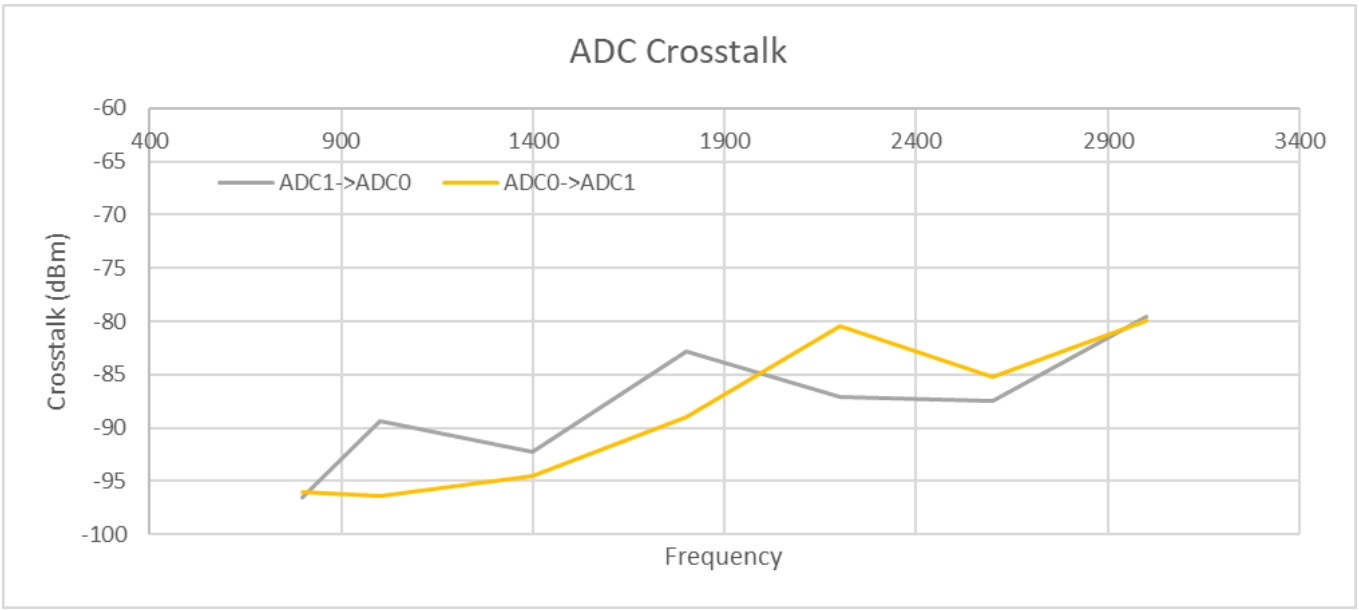

Figure 19 : ADM-XRC-9R4 ADC Crosstalk

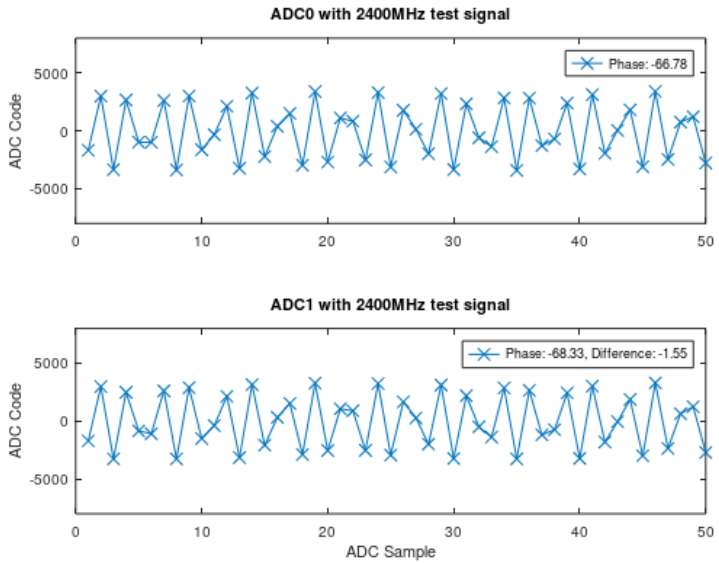

Figure 20 : ADM-XRC-9R4 ADC Phase Matching

4.7.2.2 DAC RF Performance

Measurement	Conditions/Comments	Value	Unit
Resolution		14	Bits
Sample Rate		0.5 - 10.0	GS/s
Full Scale Output	Voltage out of RF connector, 40.5mA, 50R termination	X.X	Vpk-pk
Full Scale Output	Power out of RF connector, 40.5mA, 50R termination	-6.5	dBm

Table 20 : DAC Parameters

Test Equipment

- Mini-Circuits SSG-6000 RF signal generator.
- Anritsu MS2721B spectrum analyser.

For the DAC measurements, the inverse SINC filter was OFF.

ADC measurements were taken over the range 1MHz to 4000MHz, and DAC measurements over the range 11MHz to 4000MHz. For all DACs/ADCs the result is adjusted to 0dB at 1000MHz.

Figure 21 : ADM-XRC-9R4 DAC Frequency Response

4.8 Configuration

4.8.1 Power-Up Sequence

At power-up, the PS will load the first-stage bootloader from the memory interface selected by the Boot Mode select switches.

The first stage bootloader is responsible for configuring the FPGA and PS attached interfaces.

> **Note:**
> If an over-temperature alert is detected from the System Monitor, the target **will be cleared** by pulsing its PROG signal. See Automatic Temperature Monitoring.

4.9 System Monitoring

The **ADM-XRC-9R4** has the ability to monitor temperature and voltage to maintain a check on the operation of the board. The monitoring is implemented using the Atmel AVR microcontroller.

Control algorithms within the microcontroller automatically check line voltages and on board temperatures and shares the information with the PS.

The following voltage rails and temperatures are monitored:

Monitor	*Purpose*
VPWR	Board Input Supply (either 5.0V or 12.0V)
12.0V	Board Input Supply
5.0V	Internally generated 5V supply
3.3V	Board Input Supply
3.3V	Internally generated 3.3V supply
2.5V	Digital clocks and DDR4
1.8V	Flash Memory, FPGA IO Voltage (VCCO)
0.85V	FPGA Core Supply (VccINT)
1.8V	Transceiver Power (AVCC_AUX)
1.2V	DDR4 SDRAM, memory I/O
0.85V	Block RAM and SD-FEC supply (VccBRAM)
1.2V	Transceiver Power (AVTT)
0.9V	Transceiver Power (AVCC)
0.85V	PS VCC power (PSVccINT)
Temp0	Micrcontroller on-die temperature
Temp1	Board temperature sensor on-die temperature
Temp2	FPGA on-die temperature

Table 21 : Voltage and Temperature Monitors

4.9.1 Automatic Temperature Monitoring

At power-up, the control logic sets the temperature limits and resets the LM87's over-temperature interrupt.

The temperature limits are shown in Table Temperature Limits:

	FPGA		Board	
	Min	Max	Min	Max
Commercial	0 degC	+85 degC	0 degC	+85 degC
Extended	0 degC	+100 degC	0 degC	+100 degC
Industrial	-40 degC	+100 degC	-40 degC	+100 degC

Table 22 : Temperature Limits

Note:
If any temperature limit is exceeded, the FPGA is automatically cleared. This is indicated by the Green LED (Target Configured) switching off and the two status LEDs showing a temperature fault indication.

The purpose of this mechanism is to protect the card from damage due to over-temperature. It is possible that it will cause the user application and, possibly, the host computer to "hang".

4.9.2 Microcontroller Status LEDs

LEDs D12 (Red) and D11 (Green) indicate the microcontroller status.

LEDs	*Status*
Green	Running and no alarms
Green + Red	Standby (Powered off)
Flashing Green + Flashing Red (together)	Attention - critical alarm active
Flashing Green + Flashing Red (alternating)	Service Mode
Flashing Green + Red	Attention - alarm active
Red	Missing application firmware or invalid firmware
Flashing Red	FPGA configuration cleared to protect board

Table 23 : Status LED Definitions

4.9.3 System Monitor Interfaces

There are two ways to communicate with the System Monitor to retrieve board status information on the ADM-XRC-9R4. One is through the Micro USB connector (shown in <ERROR>USB Interfaces), the other is using one of the PS UART interfaces (shown in Serial COM Ports). These communication interfaces are intended to be used with Alpha-Data utility called avr2util. Avr2util is provided with the 9R4 PetaLinux BSP, and can be run from the ADM-XRC-9R4 once booted.

To see available options, run:

```
avr2util -?
```

To display sensor values (use -psuart for the PS UART interface, or -usbcom for the MicroUSB interface):

```
avr2util -psuart /dev/ttyPS1,170000 display-sensors
```

If the user programmable clock must be re-programmed, contact support@alpha-data.com for details.

Appendix A: Rear Connector Pinouts

Appendix A.1: Primary XMC Connector, P5

.	A	B	C	D	E	F
1:	PN5_P0	PN5_N0	3V3	PN5_P1	PN5_N1	VPWR
2:	GND	GND	-	GND	GND	MRSTI_L
3:	PN5_P2	PN5_N2	3V3	PN5_P3	PN5_N3	VPWR
4:	GND	GND	TCK	GND	GND	MRSTO_L*
5:	-	-	3V3	-	-	VPWR
6:	GND	GND	TMS	GND	GND	12V0
7:	-	-	3V3	-	-	VPWR
8:	GND	GND	TDI	GND	GND	M12V0
9:	-	-	-	-	-	VPWR
10:	GND	GND	TDO	GND	GND	GA0
11:	PER_P0	PER_N0	MBIST_L*	PER_P1	PER_N1	VPWR
12:	GND	GND	GA1	GND	GND	MPRESENT_L
13:	PER_P2	PER_N2	3V3_AUX	PER_P3	PER_N3	VPWR
14:	GND	GND	GA2	GND	GND	I2C_SDA
15:	-	-	-	-	-	VPWR
16:	GND	GND	MVMRO	GND	GND	MSCL
17:	-	-	-	-	-	-
18:	GND	GND	-	GND	GND	-
19:	REFCLK0_P	REFCLK0_N	-	WAKE_L	ROOT0_L	-

Table 24 : Pn5 Interface

Appendix A.2: Secondary XMC Connector, P6

.	A	B	C	D	E	F
1:	PN6_DP_GPI-O0_N	PN6_DP_GPI-O0_P	GPIO14	PN6_DP_GPI-O1_N	PN6_DP_GPI-O1_P	GPIO8
2:	GND	GND		GND	GND	ERROR
3:	PN6_DP_GPI-O2_N	PN6_DP_GPI-O2_P		PN6_DP_GPI-O3_N	PN6_DP_GPI-O3_P	ERROR
4:	GND	GND		GND	GND	ERROR
5:	PN6_DP_GPI-O4_N	PN6_DP_GPI-O4_P	GPIO13	PN6_DP_GPI-O5_N	PN6_DP_GPI-O5_P	ERROR
6:	GND	GND	GPIO12	GND	GND	GPIO7
7:			GPIO11			GPIO6
8:	GND	GND	GPIO10	GND	GND	GPIO5
9:	-	-	GPIO9			GPIO4
10:	GND	GND		GND	GND	ERROR
11:	PN6_DP_GPI-O6_N	PN6_DP_GPI-O6_P		PN6_DP_GPI-O7_N	PN6_DP_GPI-O7_P	ERROR
12:	GND	GND		GND	GND	ERROR
13:	PN6_DP_GPI-O8_N	PN6_DP_GPI-O8_P		PN6_DP_GPI-O9_N	PN6_DP_GPI-O9_P	ERROR
14:	GND	GND		GND	GND	ERROR
15:	-	-		-	-	ERROR
16:	GND	GND		GND	GND	GPIO3
17:	-	-		-	-	GPIO2
18:	GND	GND		GND	GND	GPIO1
19:	-	-		RF_REFCLK_N	RF_REFCLK_P	GPIO0

Table 25 : Pn6 Interface

Appendix A.2.1: Pn6 GPIO Pin Map

Signal	P6 Pin	FPGA Pin	FPGA Bank
GPIO0	F19	G11	88
GPIO1	F18	F9	88
GPIO2	F17	F10	88
GPIO3	F16	E9	88
GPIO4	F9	E10	88
GPIO5	F8	D11	88
GPIO6	F7	D9	88
GPIO7	F6	A9	88
GPIO8	F1	B11	88
GPIO9	C9	E11	88
GPIO10	C8	C9	88
GPIO11	C7	A10	88
GPIO12	C6	B10	88
GPIO13	C5	C10	88
GPIO14	C1	C11	88

Table 26 : Pn6 GPIO Pin Map

Appendix A.3: PMC Connector P4

Signal	P4 Pin	P4 Pin	Signal
-	1	2	-
-	3	4	-
-	5	6	-
-	7	8	-
-	9	10	GPIO14
-	11	12	GPIO8
-	13	14	-
-	15	16	-
-	17	18	-
GPIO13	19	20	-
GPIO12	21	22	GPIO7
GPIO11	23	24	GPIO6
GPIO10	25	26	GPIO5
GPIO9	27	28	GPIO4
-	29	30	-
-	31	32	-
-	33	34	-
-	35	36	-
-	37	38	-
-	39	40	-
-	41	42	GPIO3
-	43	44	GPIO2
-	45	46	GPIO1
-	47	48	GPIO0
-	49	50	-
-	51	52	-
-	53	54	-
-	55	56	-
-	57	58	-
-	59	60	-
COM1_RXD	61	62	-
COM1_TXD	63	64	-

Table 27 : Pn4 Interface

Revision History

Date	Revision	Nature of Change	Section(s)
19 Apr 2023	0.1	Copied/updated from 9R1 user guide.	
16 May 2023	1.0	First release	
08 Jun 2023	1.1	Removed dead link to heatsink environmental specifications	ERROR

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